Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.140”**

**SOURCE**

**SOURCE**

**G**

**170”**

**Top Material: Al**

**Backside Material: Ti/Ni/Ag**

**GATE Pad Size: .016 x .020”**

**Backside Potential: DRAIN**

**APPROVED BY: DK DIE SIZE .140” X .170” DATE: 3/8/23**

**MFG: INT’L RECTIFIER THICKNESS .016” P/N: IRF1404Z**

**DG 10.1.2**

#### Rev B, 7/1